Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A pre-driver having an unbalanced output, comprising:

a first data path having a plurality of transistor output stages;

a second data path having a plurality of transistor output stages, wherein said first data path carries a data signal and said second data path carries a delayed version of said data signal; and

a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of transistor output stages in response to the level of conductivity of a subsequent driver output stage, wherein one of said pair of transistor output stages is connected to said first data path and another of said pair of transistor output stages is connected to said second data path.

2. (currently amended) A method of providing an unbalanced output drive capability to correct for output skews in subsequent amplification stages, comprising:

providing a plurality of output drive stages on a first data path and on a second data path, wherein said first data path carries a data signal and said second data path carries a delayed version of said data signal;

controlling in pairs the number of output drive stages on said first and second data paths that are activated in response to the amount of skew, said output stages including at least one pair of output drive stages wherein one output transistor of said pair is connected to said first data path and another of said pair of output transistors is connected to said second data path.

3. (original) The method of claim 2 wherein said step of controlling includes the step of generating a two-bit code and wherein said two-bit code is used to control the number of active output drive stages.

4. (currently amended) A method of providing an unbalanced output drive capability, comprising:

generating a two-bit signal representative of the relative strength of an n-channel transistor and a p-channel transistor in an output device; and

controlling the number of output pre-driver stages that are active on a first data path and on a second data path in response to said two-bit signal, wherein said first data path carries a data signal and said second data path carries a delayed version of said data signal, wherein at least a first pair of said output stages is controlled by the first bit of said two-bit signal and at least a second pair of said output stages is controlled by the second bit of said two-bit signal, and wherein one output stage of each of said pairs is connected to said first data path and another output stage of each of said pairs is connected to said second data path.

5. (currently amended) A method, comprising:

generating a signal representative of the relative strength of an n-channel transistor and a p-channel transistor in an output device;

enabling certain output stages in a pre-driver in response to said signal, wherein said pre-driver includes a first data path carrying a data signal and a second data path carrying a delayed version of said data signal, wherein said pre-driver produces an unbalanced output, and wherein at least a pair of said certain output stages is enabled in response to said signal, said pair having an output stage connected to said first data path and another output stage connected to said second data path; and

inputting a data signal to the output device through the pre-driver.

6. (currently amended) A pre-driver providing an unbalanced output drive capability, comprising:

a first data path having a plurality of output transistors;

a second data path having a plurality of output transistors, wherein said first data path carries a data signal and said second data path carries a delayed version of said data signal; and

a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of output transistors in response to signals indicative of the strength of the

output transistors in an output device, wherein one of said pair of output transistors is connected to said first data path and another of said pair of output transistors is connected to said second data path.

7. (currently amended) A portion of a data path, comprising:

an output driver responsive to a data signal; and

a pre-driver providing an unbalanced output drive capability, comprising:

a first pre-driver data path having a plurality of output transistors;

a second pre-driver data path having a plurality of output transistors, wherein said first pre-driver data path carries a data signal and said second pre-driver data path carries a delayed version of said data signal; and

a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of output transistors in response to signals indicative of the strength of output transistors in said output driver wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.

8. (currently amended) A memory device, comprising:

a plurality of memory cells arranged in an array of rows and columns;

a plurality of devices for identifying cells within said array;

a plurality of pads;

a data path connecting said plurality of pads and said array, said data path comprising:

an output driver responsive to a data signal; and

a pre-driver providing an unbalanced output drive capability, comprising:

a first pre-driver data path having a plurality of output transistors;

a second pre-driver data path having a plurality of output transistors, wherein said first pre-driver data path carries a data signal and said second pre-driver data path carries a delayed version of said data signal; and

a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of output transistors in response to signals indicative of

the strength of output transistors in said output driver wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.

9. (currently amended) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus;

an output device coupled to the processor through the processor bus;

a memory device coupled to the processor bus, said memory device comprising:

a plurality of memory cells arranged in an array of rows and columns;

a plurality of devices for identifying cells within said array;

a plurality of pads;

a data path connecting said plurality of pads and said array, said data path including:

an output driver responsive to a data signal; and

a pre-driver providing an unbalanced output drive capability, comprising:

a first pre-driver data path having a plurality of output transistors;

a second pre-driver data path having a plurality of output transistors, wherein said first pre-driver data path carries a data signal and said second pre-driver data path carries a delayed version of said data signal; and

a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of output transistors in response to signals indicative of the strength of output transistors in said output driver wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.